

**REMARKS**

Reconsideration of the above-identified application, as amended, is respectfully requested.

In the Office Action of April 14, 2005, the Examiner rejected Claims 1-4, 15-18 and 20-23 under 35 U.S.C. §102(e), as being allegedly anticipated by Funaba (U.S. Patent No. 6,853,213) (hereinafter "Funaba").

With respect to the rejection of Claims 1-4, 15-18 and 20-23 18, 19-30, 35, 36-47 and 52-55 under 35 U.S.C. §102(e), as being allegedly unpatentable over Funaba, applicant respectfully disagrees.

The present invention as set forth in independent Claims 1, 14 and 20 is directed to a low reflection driver for a high speed simultaneous bi-directional transmission line/data bus which is designed such that units at both ends of the transmission line/data bus there is configured a switching current source connected to a matching resistor in parallel. According to the invention, as the impedance of the switch current source is always much larger than the resistance of matching resistor regardless of whether the main MOSFETs providing the switching currents are in saturation mode or in cut-off mode, the resultant resistance is always equal to the resistance of the matching resistor.

It is respectfully submitted that, for a MOSFET, only when the gate-source voltage  $V_{gs}$ , the drain-source voltage  $V_{ds}$  and threshold voltage  $V_{th}$  meet  $|V_{gs}-V_{th}| < |V_{ds}|$ , the MOSFET is in saturation mode. Its behavior is like a current source because the drain current is independent of the drain-source voltage in the saturation mode. As described in the current specification, for example, at paragraphs [0034] and [0039], the invention is provisioned with means for maintaining each of the MOSFETs in saturation mode.

Being the case, the Examiner's interpretation of the device in Funaba relied upon in his rejection of independent Claim 1 is misplaced. That is, in the Office Action, the Examiner's statement that "...each of the first driver unit and the second driver unit having a sourcing current source (MP11 & R11, Fig. 1)..." is incorrect. As shown in Figure 1A, 1B of Funaba, the gate of the P-type MOSFET MP11 is connected to the digital control circuit 20, i.e., an INV (inverter circuit) output. The output voltage can thus only be of two values: 0V or VDDQ. Thus, in Funaba, when the output voltage is 0V, the P-type MOSFET is in linear mode and its behavior is like a resistor; when the output is VDDQ, the P-type MOSFET is in cut-off mode and the behavior is like an open circuit. From this, it is readily concluded that MP11 is never a current source.

Furthermore, in Funaba, each of the MOSFETs MP11 and MN11 are in series with each respective resistor R11, R12, not in parallel.

Contrarily, the present invention, as shown in Figure 2 and as claimed in Claims 1, 14 and 20, is directed to driver/receiver units for a bi-directional data bus that each comprise sourcing and sinking current sources (e.g., I1a,I2a) and resistors (e.g., R1a,R2a, respectively) in parallel, which is clearly not taught in Funaba. In view of this, the Examiner is respectfully requested to withdraw the rejection of Claims 1, 14 and 20 and all claims dependent thereon.

In view of the foregoing remarks herein, it is respectfully submitted that this application is in condition for allowance. Accordingly, it is respectfully requested that this application be allowed and a Notice of Allowance be issued. If the Examiner believes that a telephone conference with the Applicants' attorneys would be advantageous to the disposition

of this case, the Examiner is requested to telephone the undersigned, Applicants' attorney, at the following telephone number: (516) 742-4343.

Respectfully submitted,



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